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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/636,115	08/10/2000	Adrian Grah	1400.4100276	6371

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/636,115	GRAH ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *6-10 and 16-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

1. Claims 1-19 are presented for examination. Claims 6-10 and 16-19 are withdrawn from further consideration as being drawn to a non-elected invention.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. Claims 1-5 and 11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Oki (Oki), U.S. patent no. 5,870,595.

As per claim 1, Oki discloses a line card circuit [fig. 7] comprising:

an activity latch [61 buffer memory unit, fig. 2] for holding an activity flag value [the size of the available area ;col. 5, lines 8-25]; and

a logic element [83, fig. 1] operatively coupled to the activity latch to receive an incoming clock signal and to provide an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value [figures, 1 and 2; col. 4, line 58-col. 5, line 29; emphasis added, "signal 54 is generated based on an value detected by detecting unit 66 from buffer memory 61 (see col. 5, lines 8-12), and output to an AND logic circuit 83 to control an output (clock signal 80) of a clock signal 6 (see fig. 1; col. 5, lines 22-29)"].

As per claim 2, Oki discloses the activity flag value is mutually exclusive with a second activity flag value held in a second activity latch [81a, 81b, fig. 8] of a second line card circuit [col. 11, lines 56-61].

As per claim 3, Oki discloses the logic element passes the incoming clock signal as the outgoing clock signal when the activity flag value has a first value [col. 5, lines 25-29; col. 11, lines 34-37].

As per claim 4, Oki discloses the logic element blocks the incoming clock signal when the activity flag value has a second value [col. 5, lines 25-29; col. 11, lines 34-37].

As per claim 5, inherently, Oki discloses the logic element provides a static output level as the output clock signal when the activity flag value has the second value [col. 5, lines 25-29; col. 11, lines 34-37; col. 11, lines 38-47; col. 12, lines 14-21].

As to claims 11-15 basically are the operating step that are carried out by the corresponding elements in claims 1-5. Accordingly, claims 11-15 are rejected for the same reason as set forth for claims 1-5.

4. Claims 1, 3-5, 11 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Karibe et al. (Karibe), JP patent no. 64-48142.

As per claim 1', Karibe discloses a circuit comprising:

an activity latch [counter 5, fig. 1] for holding an activity flag value [abstract all]; and

a logic element [7, fig. 1] operatively coupled to the activity latch to receive an incoming clock signal and to provide an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value [figure 1; abstract all].

As per claim 3, Karibe discloses the logic element passes the incoming clock signal as the outgoing clock signal when the activity flag value has a first value [abstract all; emphasis added "has a not ZERO value"].

As per claim 4, Karibe discloses the logic element blocks the incoming clock signal when the activity flag value has a second value [abstract all; emphasis added "has a ZERO value"].

As per claim 5, inherently, Karibe discloses the logic element provides a static output level as the output clock signal when the activity flag value has the second value [abstract all].

As to claims 11 and 13-15 basically are the operating step that are carried out by the corresponding elements in claims 1 and 3-5. Accordingly, claims 11 and 13-15 are rejected for the same reason as set forth for claims 1 and 3-5.

5. Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Senoh (Senoh), US patent no. 5,914,580.

Senoh is a prior art cited in prior office action.

As per claim 1, Senoh discloses a circuit [fig. 2] comprising:

an activity latch [10, fig. 2] for holding an activity flag value [col. 4, lines 45-53]; and

a logic element [11, fig. 2] operatively coupled to the activity latch to receive an incoming clock signal and to provide an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value [figures, 1; col. 5, lines 15-26].

As to claim 11 basically is the operating step that are carried out by the corresponding elements in claim 1. Accordingly, claim 11 is rejected for the same reason as set forth for claim 1.

6. Applicant's arguments filed on 3/21/2005 have been fully considered but are moot in view of new ground(s) of rejection.

7. In the remarks, applicants argued in substance that in **Oki** system fails to disclose an activity latch for holding an activity flag value; and **Karibe** fails to disclose an activity latch of a line card.

8. The examiner respectfully traverses. In **Oki** system discloses an activity latch for holding an activity flag value [61, fig. 2; col. 5, lines 8-25]. **Karibe** discloses an activity latch of a line card [fig. 2] for holding an activity flag value [counter 5; abstract all]. Also see rejection above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

May 31, 2005